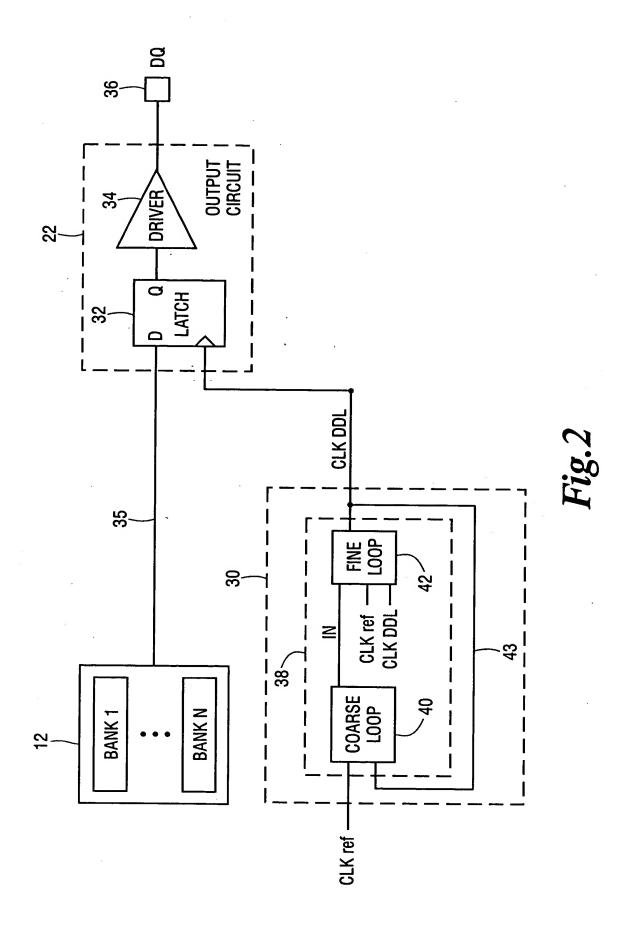
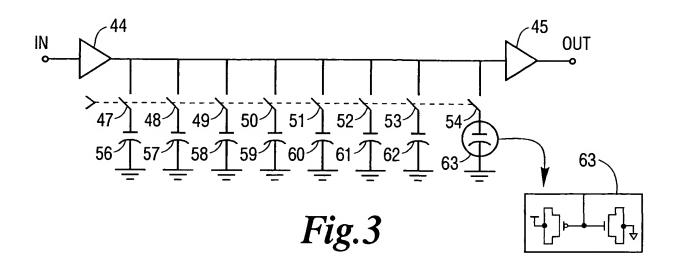


Fig. 1



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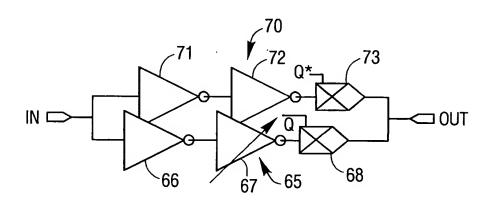


Fig.4

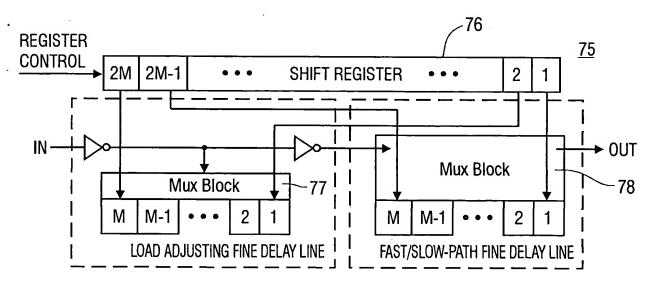


Fig.5

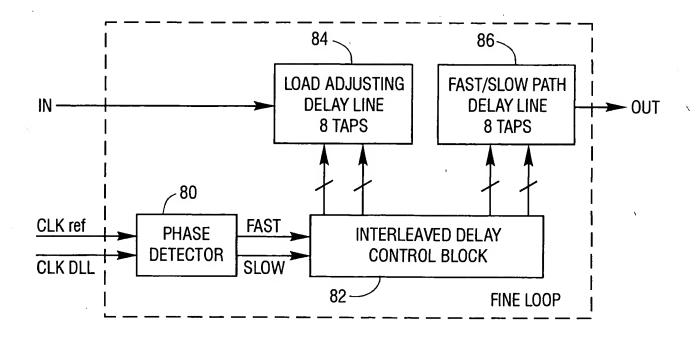
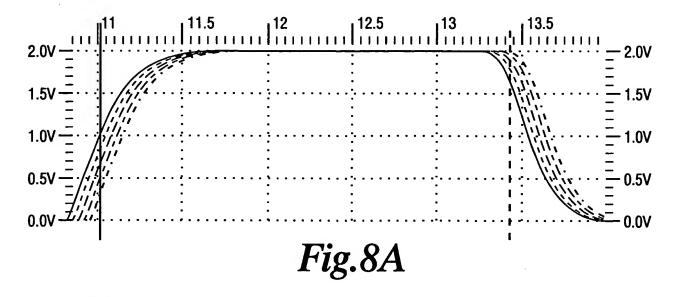
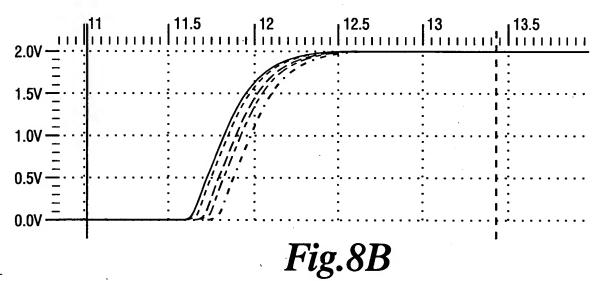
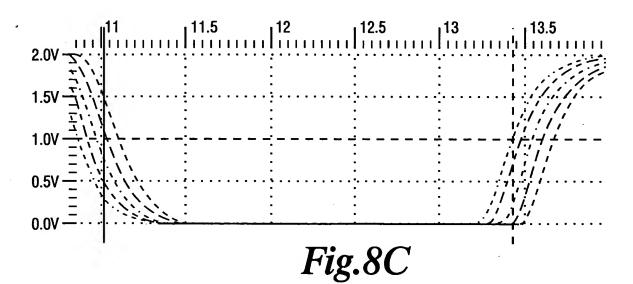


Fig.6 OUT IN  $\mathcal{E}_{n}$ 91 90 - 92 93 Fig.7A 80 CLK ref FAST PHASE SELECTION CONTROL BLOCK DETECTOR CLK DLL SLOW 88

Fig.7







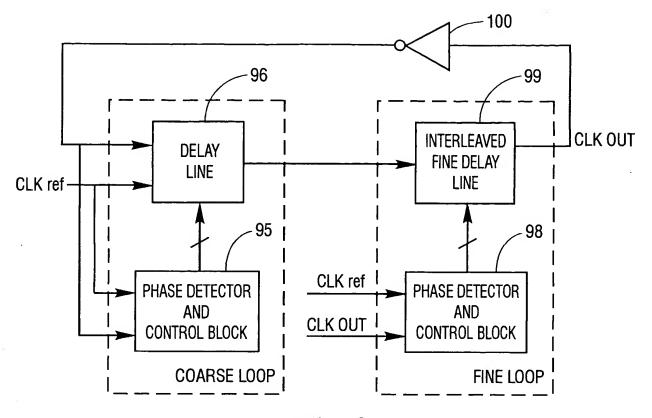


Fig.9

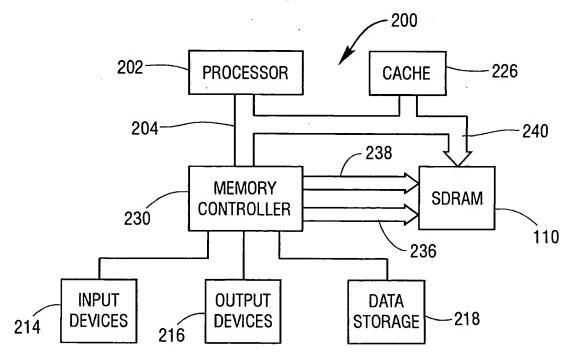


Fig.10